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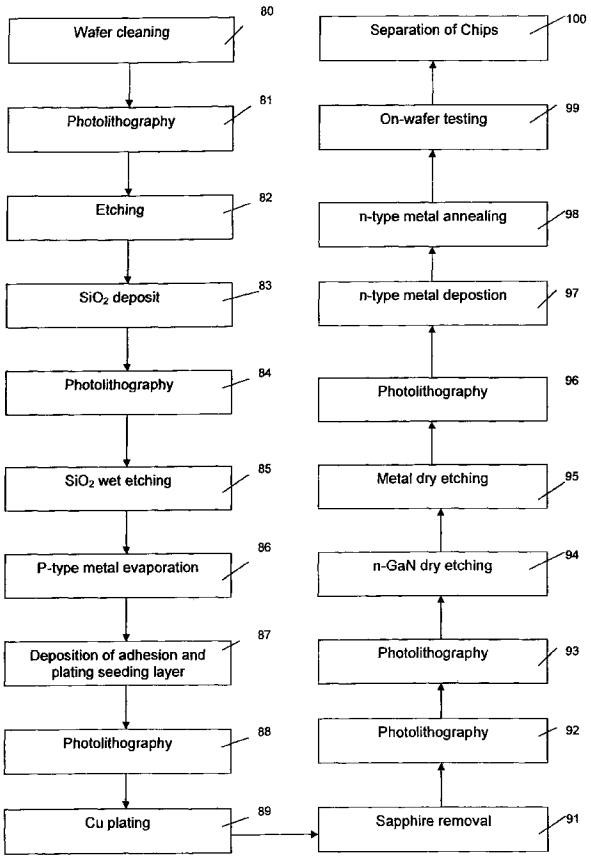
(54) Title: FABRICATION OF REFLECTIVE LAYER ON SEMICONDUCTOR LIGHT EMITTING DIODES



(57) Abstract: Fabrication of Reflective Layer on Semiconductor Light emitting diodes A method for fabrication of a reflective layer on a semiconductor light emitting diode, the semiconductor light emitting diode having a wafer with multiple epitaxial layers on a substrate; the method comprising applying a first ohmic contact layer on a front surface of the multiple epitaxial layers, the first ohmic contact layer being of a reflective material to also act as a reflective layer.

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Fabrication of Reflective Layer on Semiconductor Light Emitting Diodes

Field of the Invention

The present invention relates to the fabrication of a reflective layer on semiconductor light emitting diodes and particularly, though not exclusively, to such a method and light emitting diode where the reflective layer acts also as the ohmic contact to the front surface of the light emitting diode.

Background to the Invention

Light emitting diodes have been recently used in large volume in mobile handsets, digital cameras, personal digital assistants, traffic lights, automobiles, and so forth. Higher brightness is required before light emitting diodes can be used for other applications such as, for example, general illumination, as the brightness of the emitted light is not sufficient for light emitting diodes to be used in such applications.

There are a few reasons why the brightness and output power of light emitting diodes is limited. One of the major reasons is the limited light extraction efficiency. Due to total reflection at the interface between light emitting diode surfaces (semiconductor), or plastic encapsulation of a light emitting diode, the external efficiency of most light emitting diodes is limited to a few percent of input electrical power, while the internal efficiency is often as high as over 90%. The internal quantum efficiency characterises how many photons are generated for each electron passing through the light emitting diode. The extraction efficiency is the percentage of the generated light that escapes from the semiconductor light emitting diode.

Various methodologies have been developed to improve the light extraction efficiency, including:

(a) surface texturing (I. Schnitzer and E. Yablonovitch, C. Caneau, T. J. Gmitter, and A. Schere, Applied Physics Letters, Volume 63, page 2174, October 1993);

(b) replacing the absorbing substrate with a non-absorbing substrate (F. A. Kish, F. M. Steranka, D. C. DeFevere, D. A. Vanderwater, K.

G. Park, C. P. Kuo, T. D. Osentowski, M. J. Peanasky, J. G. Yu, R. M. Fletcher, D. A. Steigerwald, M. G. Craford, and V. M. Robbins, Applied Physics Letters, volume 64, page 2839 ,1994);

(c) providing a mirror on or within the substrate (R. H. Horng, D.S. Wuu, S. C. Wei, C. Y. Tseng, M. F. Huang, K. H. Chang, P. H. Liu, K. C. Lin, Applied Physics Letters, Volume 75, page 3054, November 1999) by wafer bonding or eutectic bonding;

(d) changing the chip geometry; and

(e) growing a semiconductor distributed Bragg reflector mirror (H. Sugawara, H. Itaya, G. Hatakoshi, Journal of Applied Physics, Volume 74, page 3189, 1993);

and so forth.

The reflective layer is normally on the rear surface – the surface to which the substrate is attached. This is because the ohmic contacts to the semiconductor are normally made on the front surface (especially for GaN light emitting diodes on a sapphire substrate), and light is emitted from the front surface and the edges of the substrate. To make this reflective layer requires a number of process steps. This is inefficient. Often the reflective layer reacts with the semiconductor layer and the solder materials, and adhesion of the reflective mirror layer to the underlying semiconductor is also a problem.

For GaN-based and AlGaInP light emitting diodes, the substrates are not good thermal conductive materials, and it is desirable to remove the substrate. In addition, the removal of the substrate simplifies the device fabrication with reflection mirrors, since the reflection mirror is on the front surface of the semiconductor, not on the back surface of the substrate, and acts also as the ohmic contact to the semiconductor front surface.

GaN blue laser performance is also improved by the removal of the substrate (W. S. Wong, M. A. Kneissl, US Patent 6,627,921 B2). Bonding the semiconductor epitaxial layers, either before or after the removal of the substrate from the semiconductor expitaxial layers, to a mechanical support (new substrate) by using eutectic bonding, wafer bonding, or by using organic bonding material, complicates the process and may limit the yield and throughput of the production. Often the bonding must be done at elevated temperatures. This may cause additional problems. For GaN light emitting diodes it is difficult to remove the sapphire

substrate for the whole wafer and keep the epitaxial layer intact, making it difficult for large volume manufacturing by using bonding methods. This is because the bonding methods do not provide intimate and homogeneous bonding between the epitaxial layers and the new mechanical substrate, and the warping of the epitaxial layers on the new substrate causes cracks or stress in the epitaxial layers.

Summary of the Invention

In accordance with a preferred form there is provided a method for fabrication of a reflective layer on a semiconductor light emitting diode, the semiconductor light emitting diode being made from a wafer with multiple epitaxial layers on a substrate; the method comprising applying a first ohmic contact layer on a front surface of the multiple epitaxial layers, the first ohmic contact layer being of a reflective material to also act as a reflective layer at its interface with the front surface.

The method may also include:

(a) applying to a front surface of the first ohmic contact layer a seed layer of a thermally conductive metal;

(b) electroplating a relatively thick layer of the thermally conductive metal on the seed layer; and

(c) removing the substrate.

The first ohmic contact layer may be coated with an adhesion layer prior to application of the seed layer.

The seed layer may be patterned with photoresist patterns before the electroplating step, the electroplating of the relatively thick layer being between the photoresist patterns. Between steps (b) and (c) there may be performed the additional step of annealing the wafer to improve adhesion. The photoresist patterns may be of a height of at least 50 micrometers, a thickness in the range 3 to 500 micrometers, and a spacing of 300 micrometers.

The seed layer may be electroplated without patterning, patterning being performed subsequently. Patterning may be by photoresist patterning and then wet etching; or by laser beam micro-machining of the relatively thick layer. The relatively thick layer may be of a height no greater that the photoresist height.

Alternatively, the relatively thick layer of thermally conductive metal may electroplated to a height greater than the photoresist and is subsequently thinned. Thinning may be by polishing.

After step (c) there may be included an extra step of forming on a rear surface of the epitaxial layers a second ohmic contact layer, the second ohmic contact layer being selected from the group consisting of: opaque, transparent, and semi-transparent. The second ohmic contact layer may be blank or patterned. Bonding pads may be formed on the second ohmic contact layer.

After step (c) ohmic contact formation and subsequent process steps may be carried out, the subsequent process steps including deposition of wire bond pads. The exposed rear surface of the epitaxial layer may be cleaned and etched before the second ohmic contact layer is deposited. The second ohmic contact layer may not cover the whole area of the second surface of the epitaxial layers.

After forming the second ohmic contact layer there is included testing of the light emitting devices on the wafer, and separating the wafer into individual devices. The light emitting devices may be fabricated without one or more selected from the group consisting of: lapping, polishing and dicing.

The first ohmic contact layer may be on p-type layers of the epitaxial layers, and the second ohmic contact layer may be formed on n-type layers of the expitaxial layers.

Dielectric films may be deposited on the epitaxial layers, openings cut in the dielectric films and second ohmic contact layer, and bond pads deposited on the epitaxial layers.

After step (c), electroplating of a thermally conductive metal on the epitaxial layers may be performed.

The thermally conductive metal may be copper, and the epitaxial layers may be multiple GaN-related layers.

In a further aspect, there is provided a light emitting device comprising epitaxial layers, a first ohmic contact layer on a front surface of the epitaxial layers, the first

ohmic contact layer being of a reflective material and, at its interface with the epitaxial layers, acts as a mirror.

There may also be an adhesive layer on the first ohmic contact layer, a seed layer of a thermally conductive metal on the adhesive layer, and a relatively thick layer of the thermally conductive metal on the seed layer. The relatively thick layer may one or more of: a heat sink, an electrical connector, and a mechanical support.

A second ohmic contact layer may be provided on a rear surface of the epitaxial layers; the second ohmic contact layer being a thin layer in the range of from 3 to 500 nanometers.

The second ohmic contact layer may also comprise bonding pads and may be selected from the opaque, transparent, and semi-transparent.

There may be an adhesive layer on the first ohmic contact layer between the first ohmic contact layer and the relatively thick layer, and a seed layer of the thermally conductive metal between the adhesive layer and the relatively thick layer. The relatively thick layer may be at least 50 micrometers thick.

The light emitting device may be: a light emitting diode or a laser diode.

Brief Description of the Drawings

In order that the invention may be better understood and readily put into practical effect there shall now be described by way of non-limitative example only a preferred embodiment of the present invention, the description being with reference to the accompanying illustrative (and not to scale) drawings in which:

Figure 1 is a schematic representation of a light emitting device at a first stage in the fabrication process;

Figure 2 is a schematic representation of the light emitting device of Figure 1 at a second stage in the fabrication process;

Figure 3 is a schematic representation of the light emitting device of Figure 1 at a third stage in the fabrication process;

Figure 4 is a schematic representation of the light emitting device of Figure 1 at a fourth stage in the fabrication process;

Figure 5 is a schematic representation of the light emitting device of Figure 1 at a fifth stage in the fabrication process;

Figure 6 is a schematic representation of the light emitting device of Figure 1 at a sixth stage in the fabrication process;

Figure 7 is a schematic representation of the light emitting device of Figure 1 at the seventh stage in the fabrication process; and

Figure 8 is a flow chart of the process.

Detailed Description of the Preferred Embodiment

For the following description, the reference numbers in brackets refer to the process steps in Figure 8.

To refer to Figure 1, there is shown the first step in the process – the metallization on the p-type surface of the wafer 10.

The wafer 10 is an epitaxial wafer with a substrate and a stack of multiple epitaxial layers 14 on it. The substrate 12 can be, for example, sapphire, GaAs, InP, Si, and so forth. Henceforth a GaN sample having GaN layer(s) 14 on sapphire substrate 12 will be used as an example. The epitaxial layers 14 (often called epilayers) are a stack of multiple layers, and the lower part 16 (which is grown first on the substrate) is usually n-type layers and the upper part 18 is often p-type layers.

On the front or top surface of GaN layers 14 is a first ohmic contact layer 20 of a reflective material and having multiple metal layers. As the front surface is relatively smooth and as first ohmic contact layer has metal layers, it is reflective. Therefore, additional process steps are not required to fabricate the reflective layer. To ohmic contact layer 20 is added an adhesion layer 22, and a thin copper seed layer 24 (Figure 2) (step 88) of a thermally conductive metal such as, for example, copper. The thermally conductive metal is preferably also electrically conductive. The stack of adhesion layers may be annealed after formation.

The first ohmic layer 20 may be a stack of multiple layers deposited and annealed on the epitaxial surface. It may not be part of the original wafer. For GaN, GaA, and InP devices, the epitaxial wafer often contains an active region that is sandwiched between n-type and p-type semiconductors. In most cases the top layer is p-type.

As shown in Figure 3, using standard photolithography (89), the thin copper seed layer 24 is patterned with relatively thick photoresists 26. The photoresist patterns 26 are of a height of at least 50 micrometers, preferably in the range 50 to 300 micrometers, more preferably 200 micrometers; and with a thickness of about 3 to 500 micrometers. They are preferably separated from each other by a spacing of about 300 micrometers, depending on the design of the final chips. The actual pattern depends on device design.

A patterned layer 28 of copper is then electroplated onto layer 24 (90) between photoresists 26 to form a heat sink that forms a part of the substrate. The copper layer 28 is preferably of a height no greater than that of the photoresists 26 and is therefore of the same or lesser height than the photoresists 26. However, the copper layer 28 may be of a height greater than that of the photoresists 26. In such a case, the copper layer 28 may be subsequently thinned to be of a height no greater than that of the photoresists 26. Thinning may be by polishing or wet etching. The photoresists 26 may or may not be removed after the copper plating. Removal may be by a standard and known method such as, for example, resin in the resist stripper solution, or by plasma aching.

Depending on the device design, processing of the epitaxial layers 14 follows using standard processing techniques such as, for example, cleaning (80), lithography (81), etching (82), device isolation (83), passivation (84), metallization (85), thermal processing (86), and so forth. (Figure 4). The wafer 10 is then annealed (87) to improve adhesion.

The epitaxial layer 14 is usually made of n-type layers 16 on the original substrate 12; and p-type layers on the original front or top surface 18 which is now covered with the ohmic layer 20, adhesion layer 22, copper seed layer 24, and the electroplated thick copper layer 28.

In Figure 5, the original substrate layer 12 is then removed (91) using, for example, the method of Kelly [M.K. Kelly, O. Ambacher, R. Dimitrov, R. Handschuh, and M. Stutzmann, phys. stat. sol. (a) 159, R3 (1997)]. The substrate may also be removed by polishing or wet etching.

Figure 6 is the penultimate step and is particularly relevant for light emitting diodes where a second ohmic contact layer 30 is added on the rear surface of, (or beneath), epitaxial layers 14, for light emission. Bonding pads 32 are also added. The second ohmic contact layer 30 is preferably transparent or semi-transparent. It is more preferably a thin layer and may be in the range of 3 to 50 nm thick.

Prior to adding second ohmic contact layer 30, known preliminary processes may be performed. These may be , for example, photolithography (92, 93), dry etching (94, 95), and photolithography (96).

Annealing (98) may follow the deposition of second ohmic contact layer 30.

The chips/dies are then tested (99) by known and standard methods. The chips/dies can then be separated (100) (Figure 7) into individual devices/chips 1 and 2 without lapping/polishing the substrate, and without dicing. Packaging follows by standard and known methods.

The top surface of the epitaxial layer 14 is preferably in the range of about 0.1 to 2.0 microns, preferably about 0.3 microns, from the active region. As the active region of the light emitting diode chip in this configuration is close to a relatively thick copper pad 28, the rate of heat removal is improved over the sapphire configuration.

Additionally or alternatively, the relatively thick layer 28 may be used to provide mechanical support for the chip. It may also be used to provide a path for heat removal from the active region of the light emitting device chip, and may also be used for electrical connection.

The plating step is performed at the wafer level (i.e., before the dicing operation) and may be for several wafers at the one time.

The first ohmic contact layer 20, being metal and relatively smooth, is quite shiny and therefore highly reflective of light. As such the first ohmic contact layer 20, at its interface with the front surface of epitaxial layers 14, also acts as a reflective surface, or mirror, to improve light output. This is achieved without additional fabrication steps. The ohmic contact layer/reflective layer 20 may be of a pure

metal or a stack of multiple metal layers, for example, Ni/Au, Ru/Au, Indium Tin Oxide (ITO), Ta/Ti, and so forth.

Although the preferred embodiments refer to the use of copper, any other platable material may be used provided it is electrically and/or heat conductive, or provides the mechanical support for the light emitting device.

By combining the reflection mirror layer formation and ohmic contact formation in a single step, the problem of bonding to another substrate is avoided. Electroplating of copper or other thermally and electrically conductive materials (e.g. metals) on the reflective mirror/ohmic contact layer is preferably at room temperature. This avoids the elevated temperatures used in present bonding processes. The relatively thick electroplated layer may be, for example, 250 micron thick. As such, it may serve as a mechanical support, thermal conductor, and an electrical conductor, thus making the removal of the original substrate somewhat easier.

Preferably, each light emitting diode die is isolated from other dies before the removal of the substrate, thus any warping or bending of the whole wafer during or after the removal of the substrate does not cause stress or cracks in individual light emitting diode dies. Since the relatively thick layer is electrically conductive, current can flow from on side of the die to the other. As a result, only one bonding wire is required. Most GaN-based light emitting diodes are on the market require two-wire bonding, as the sapphire is an insulator.

Whilst there has been described in the foregoing description a preferred form of the present invention, it will be understood by those skilled in the technology that many variations or modifications in design, construction or operation may be made without departing from the present invention.

The claims:

1. A method for fabrication of a reflective layer on a semiconductor light emitting diode, the semiconductor light emitting diode being made from a wafer with multiple epitaxial layers on a substrate; the method comprising applying a first ohmic contact layer on a front surface of the multiple epitaxial layers, the first ohmic contact layer being of a reflective material to also act as a reflective layer at its interface with the front surface.

2. A method as claimed in claim 1 further comprising:
   (a) applying to a front surface of the first ohmic contact layer a seed layer of a thermally conductive metal;
   (b) electroplating a relatively thick layer of the thermally conductive metal on the seed layer; and
   (c) removing the substrate.

3. A method as claimed in claim 2, wherein the first ohmic contact layer is coated with an adhesion layer prior to application of the seed layer.

4. A method as claimed in claim 2 or claim 3, wherein the seed layer is patterned with photoresist patterns before the electroplating step (b), the electroplating of the relatively thick layer being between the photoresist patterns.

5. A method as claimed in any one of claims 2 to 4, wherein between steps (b) and (c) there is performed the additional step of annealing the wafer to improve adhesion.

6. A method as claimed in claim 4, wherein the photoresist patterns are of a height of at least 50 micrometers.

7. A method as claimed in claim 4, wherein the photoresist patterns have a thickness in the range 3 to 500 micrometers.

8. A method as claimed in any one of claims 4, 6 and 7, wherein the photoresist patterns have a spacing of 300 micrometers.

9. A method as claimed in any one of claims 2 to 8, wherein the seed layer is electroplated in step (b) without patterning, patterning being performed subsequently.

10. A method as claimed in claim 9, wherein patterning is by one of: photoresist patterning and then wet etching, and laser beam micro-machining of the relatively thick layer.

11. A method as claimed in any one of claims 4 to 10, wherein the relatively thick layer is of a height no greater that the photoresist height.

12. A method as claimed in any one of claims 4 to 10, wherein the relatively thick layer of thermally conductive metal is electroplated to a height greater than the photoresist and is subsequently thinned by polishing.

13. A method as claimed in any one of claims 1 to 12, wherein after step (c) there is included an extra step of forming on a rear surface of the epitaxial layers a second ohmic contact layer, the second ohmic contact layer being selected from the group consisting of: opaque, transparent, and semi-transparent; the second ohmic contact layer being one of blank and patterned.

14. A method as claimed in claim 13, wherein at least one bonding pad is formed on the second ohmic contact layer.

15. A method as claimed in any one of claims 2 to 12, wherein after step (c) ohmic contact formation and subsequent process steps are carried out, the subsequent process steps including deposition of at least one wire bond pad.

16. A method as claimed in claim 15, wherein the exposed epitaxial layer is cleaned and etched before the second ohmic contact layer is deposited.

17. A method as claimed in any one of claims 13 to 16, wherein the second ohmic contact layer does not cover the whole area of the second surface of the epitaxial layers.

18. A method as claimed in any one of claims 15 to 17, wherein after forming the second ohmic contact layer there is included testing of the light emitting devices on the wafer, and separating the wafer into individual devices.

19. A method as claimed in any one of claims 1 to 18, wherein the light emitting devices are fabricated without one or more selected from the group consisting of: lapping, polishing and dicing.

20. A method as claimed in any one of claims 1 to 19, wherein the first ohmic contact layer is on p-type layers of the epitaxial layers.

21. A method as claimed in any one of claims 13 to 18, wherein the second ohmic contact layer is formed on n-type layers of the expitaxial layers.

22. A method as claimed in claim 13, wherein after step (c), dielectric films are deposited on the epitaxial layers, openings are cut in the dielectric films and second ohmic contact layer, and bond pads deposited on the epitaxial layers.

23. A method as claimed in any one of claims 2 to 12, wherein after step (c), electroplating of a thermally conductive metal on the epitaxial layers is performed.

24. A method as claimed in any one of claims 2 to 23, wherein the thermally conductive metal comprises copper and the epitaxial layers comprise multiple GaN-related layers.

25. A light emitting diode fabricated by the method of any one of claims 1 to 24.

26. A semiconductor light emitting diode comprising epitaxial layers, a first ohmic contact layer on a front surface of the epitaxial layers, the first ohmic contact layer being of a reflective material and, at its interface with the epitaxial layers, acts as a mirror.

27. A light emitting diode as claimed in claim 26, further comprising an adhesive layer on the first ohmic contact layer, a seed layer of a thermally

conductive metal on the adhesive layer, and a relatively thick layer of the thermally conductive metal on the seed layer, the relatively thick layer being one or more selected from the group consisting of: a heat sink, an electrical connector, and a mechanical support.

28. A light emitting diode as claimed in claim 26 or claim 27, further comprising a second ohmic contact layer on a rear surface of the epitaxial layers; the second ohmic contact layer being a thin layer in the range of form 3 to 500 nanometers.

29. A light emitting diode as claimed in claim 28, wherein the second ohmic contact layer comprises bonding pads and is selected from the group consisting of: opaque, transparent, and semi-transparent.

30. A light emitting diode as claimed in any one of claims 26 to 29, wherein the thermally conductive metal comprises copper; and the epitaxial layers comprise GaN-related layers.

31. A light emitting diode as claimed in any one of claims 26 to 30, wherein there is an adhesive layer on the first ohmic contact layer between the first ohmic contact layer and the relatively thick layer, and a seed layer of the thermally conductive metal between the adhesive layer and the relatively thick layer.

32. A light emitting diode as claimed in any one of claims 26 to 31, wherein the relatively thick layer is at least 50 micrometers thick.

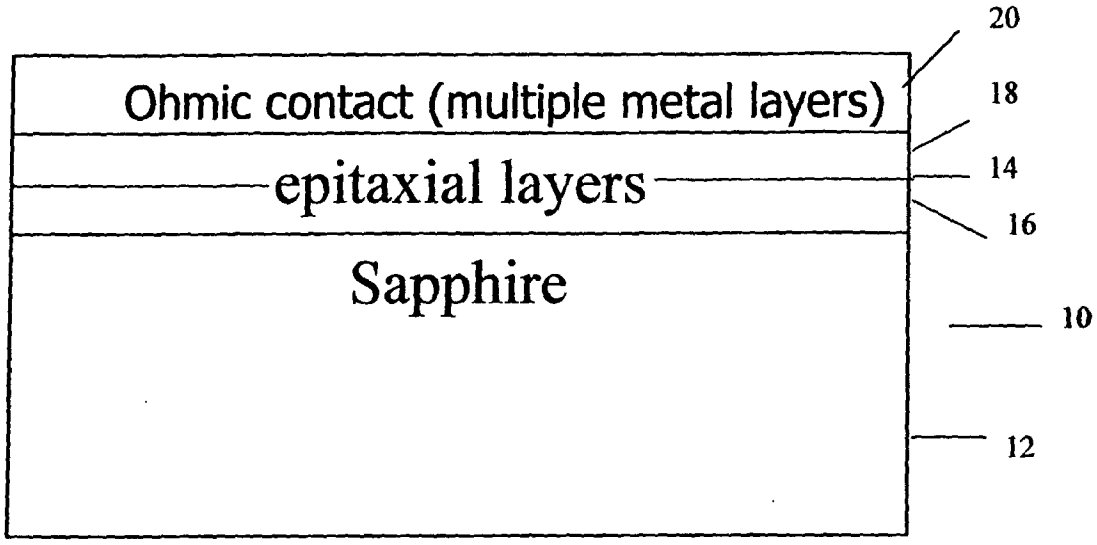

Figure 1

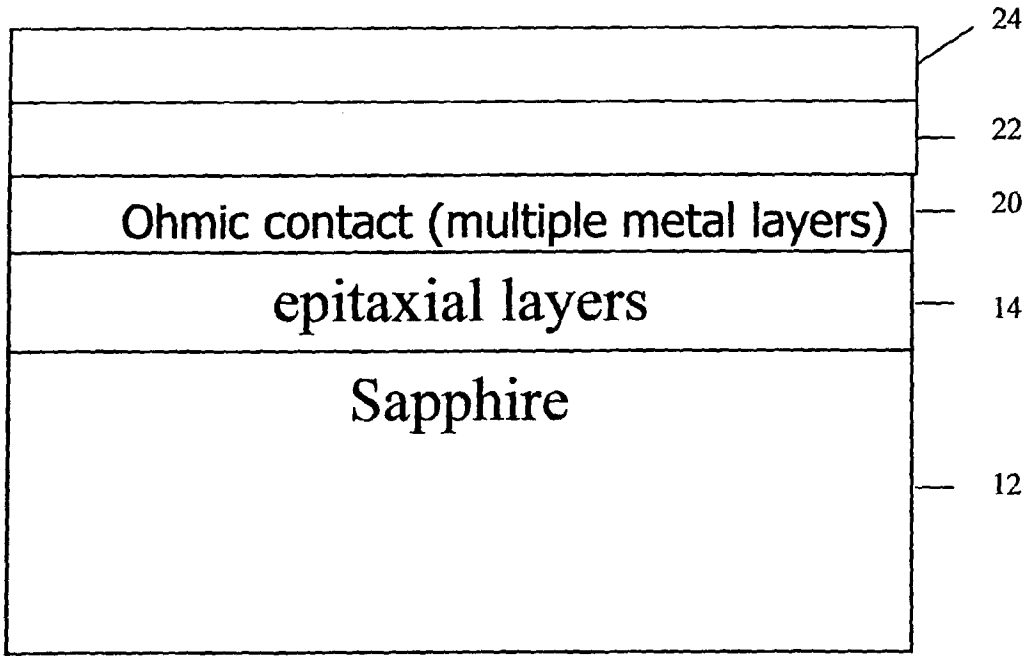

Figure 2

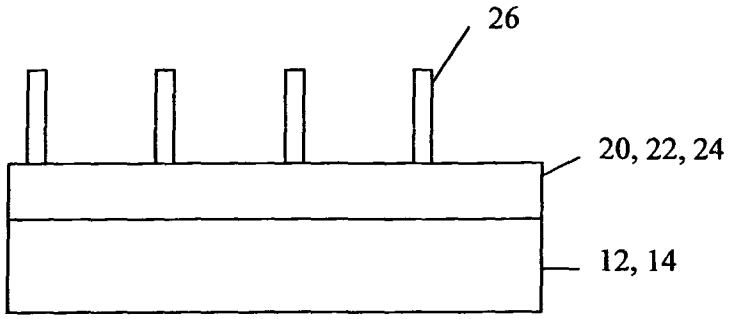

Figure 3

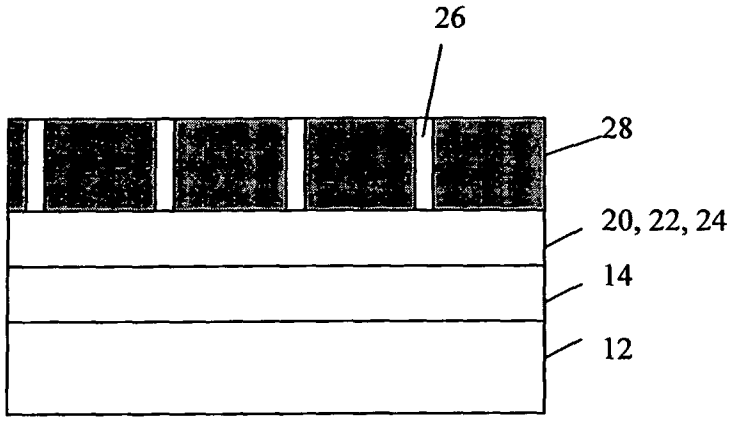

Figure 4

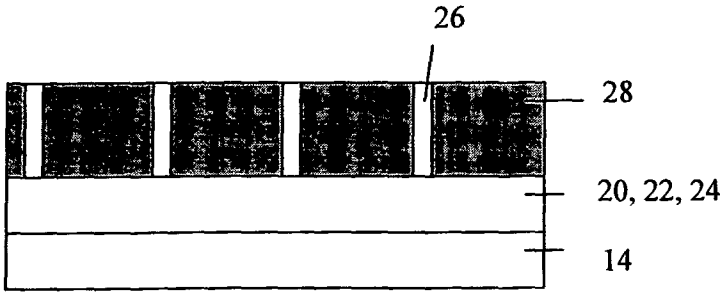

Figure 5

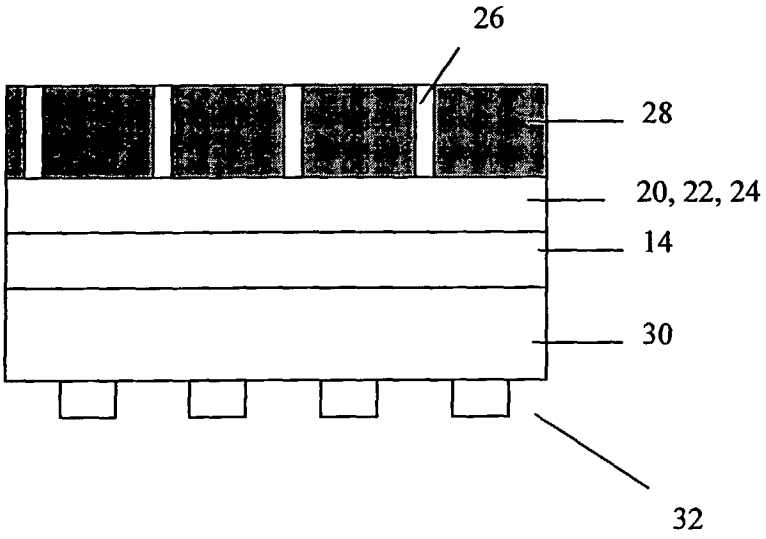

Figure 6

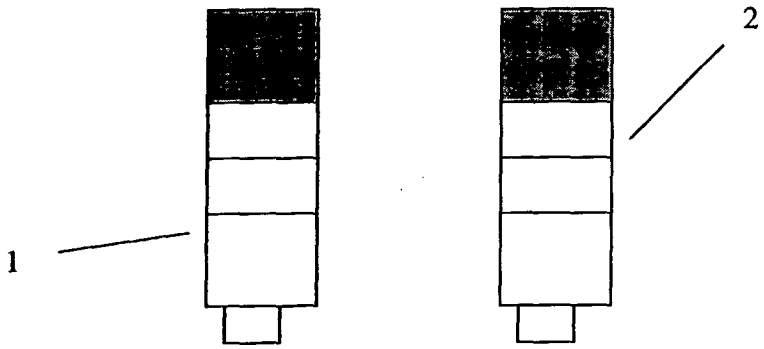

Figure 7

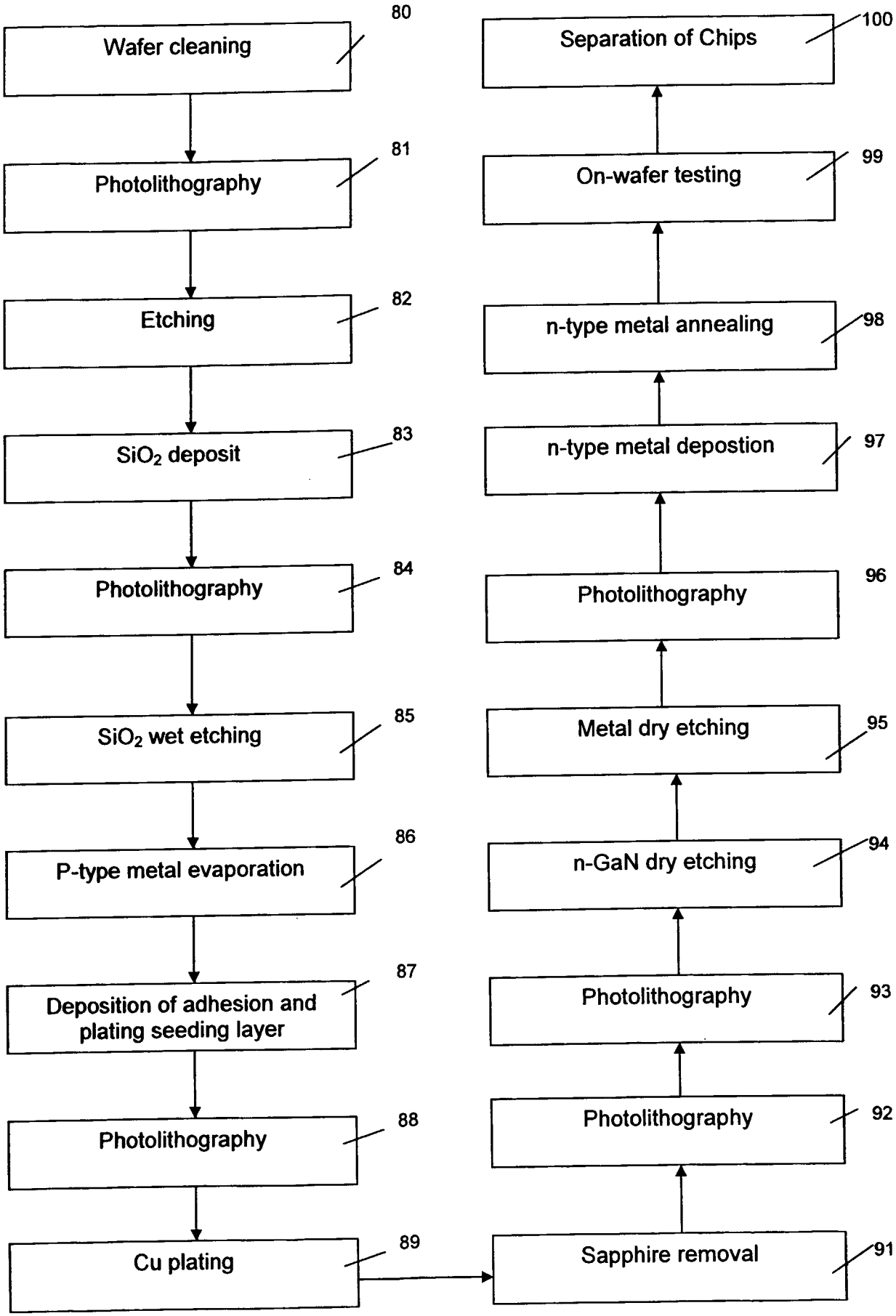
Wafer cleaning
80
Photolithography
81
Etching
82
SiO_2 deposit
83
Photolithography
84
SiO_2 wet etching
85
P-type metal evaporation
86
Deposition of adhesion and plating seeding layer
87
Photolithography
88
Cu plating
89
Sapphire removal
91
Photolithography
92
Photolithography
93
n-GaN dry etching
94
Metal dry etching
95
Photolithography
96
n-type metal depostion
97
n-type metal annealing
98
On-wafer testing
99
Separation of Chips
100

Figure 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2005/000062

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl. [7]: H01L 33/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
DWPI and JAPIO: H01L 33/-, LED, reflect, layer,film,contact,electrode,ohmic,reflect,conduct,metal,epilayer,epitaxial, roughen, remove, texture

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/0179910 A (SLATER,JR) 5 December 2002 See para [0056].	1,20,25,26,28
X	US 6 573 537 B (STEIGERWALD et al) 3 June 2003 See col 14 lines 48-59.	1-32

☐ Further documents are listed in the continuation of Box C ☒ See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
6 May 2005	12 MAY 2005
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. (02) 6285 3929	Authorized officer **S. T. PRING** Telephone No : (02) 6283 2210

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
US	2002/0179910	AU	63916/99	CA	2343416	CA	2 465 228
		CN	1 323 446	EP	1 125 320	EP	1 440 460
		MX	PA01002751	US	6 803 243	US	6 884 644
		US	2004171204	WO	2000/16382	WO	2003/038877
US	6 573 537	AU	27389/01	DE	102 13 701	EP	1 161 772
		JP	2001/237458	JP	2002/335014	US	6 514 782
		WO	2001/47039				

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

END OF ANNEX